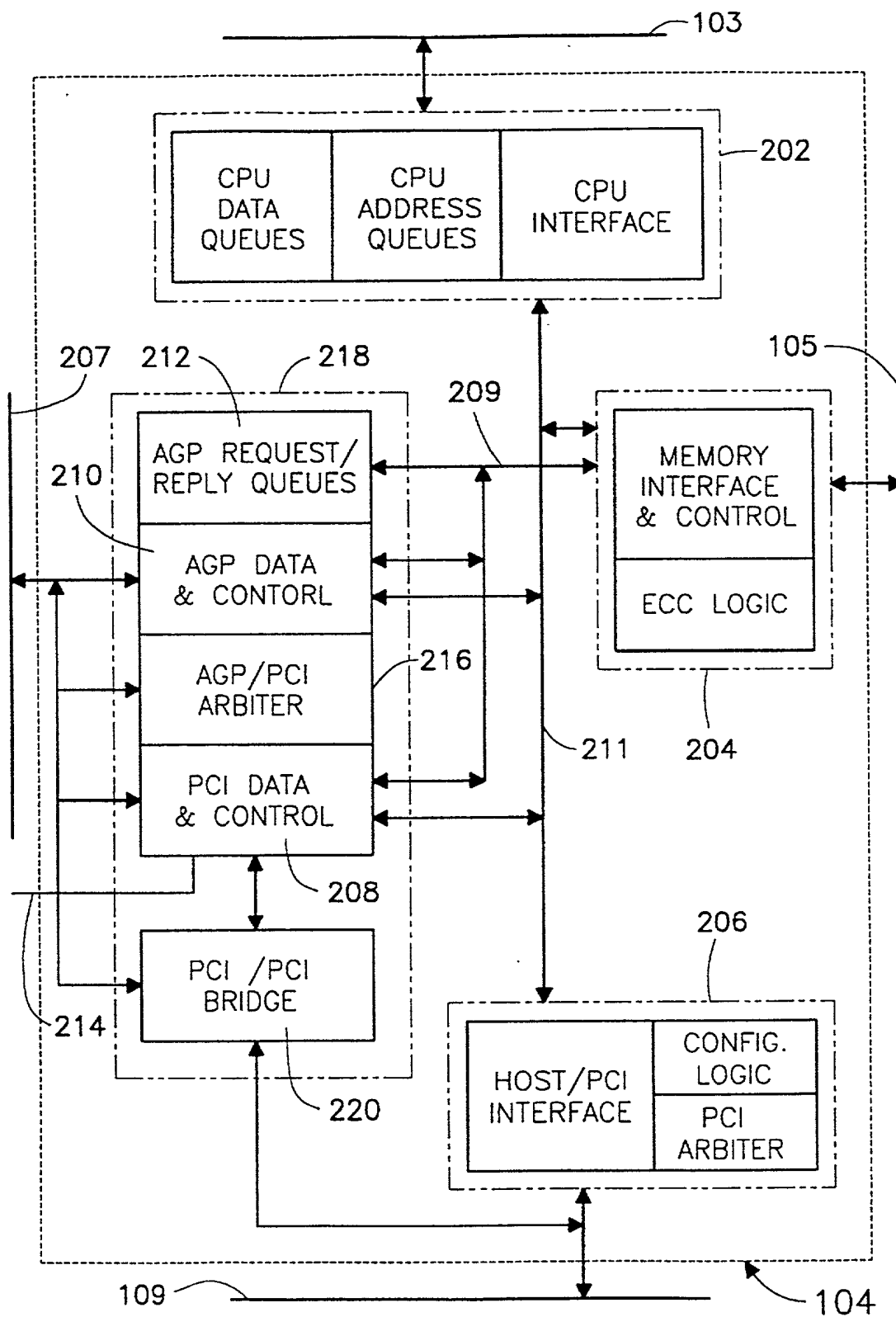


FIG. 1



**FIGURE 2**

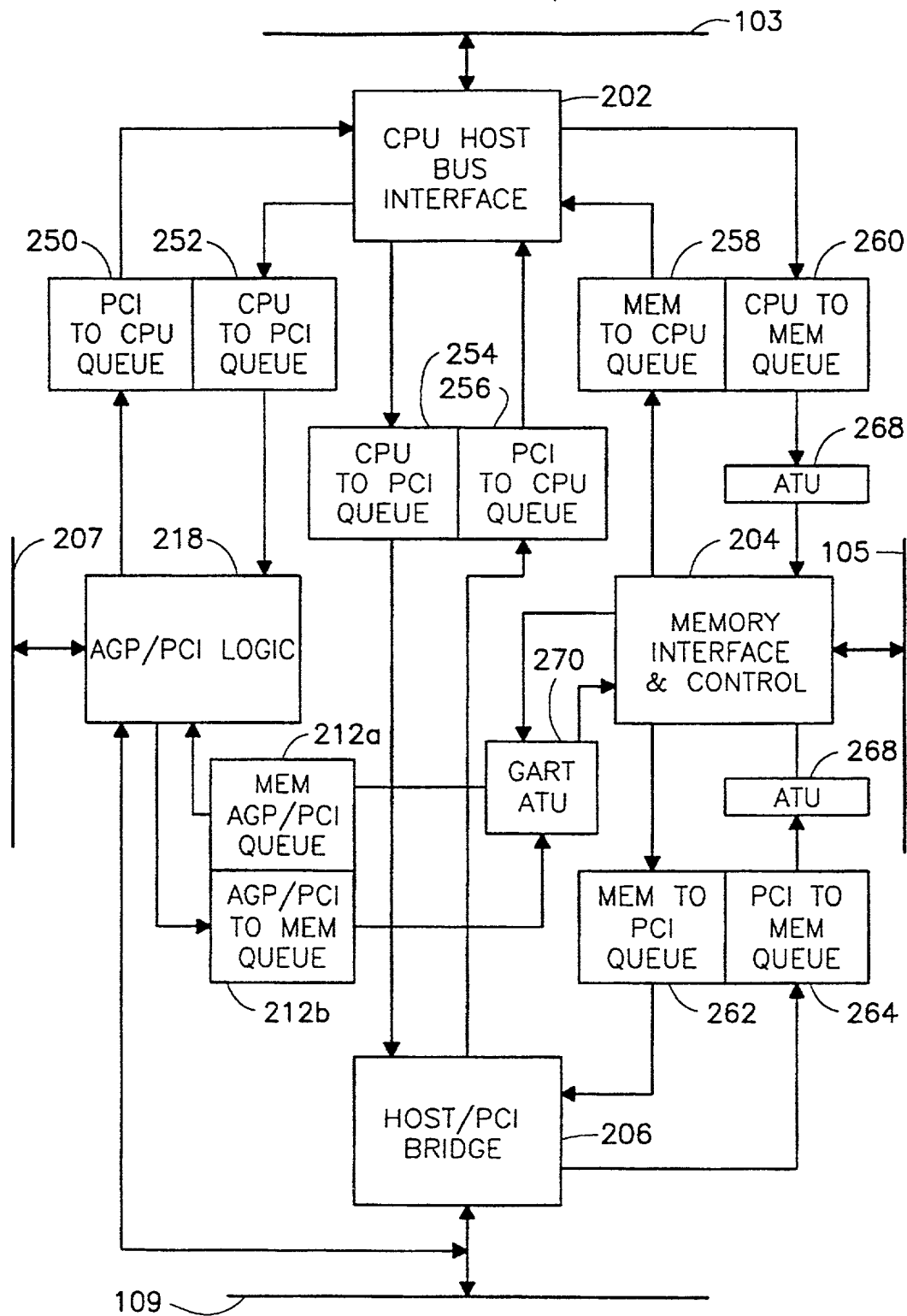


FIGURE 2A

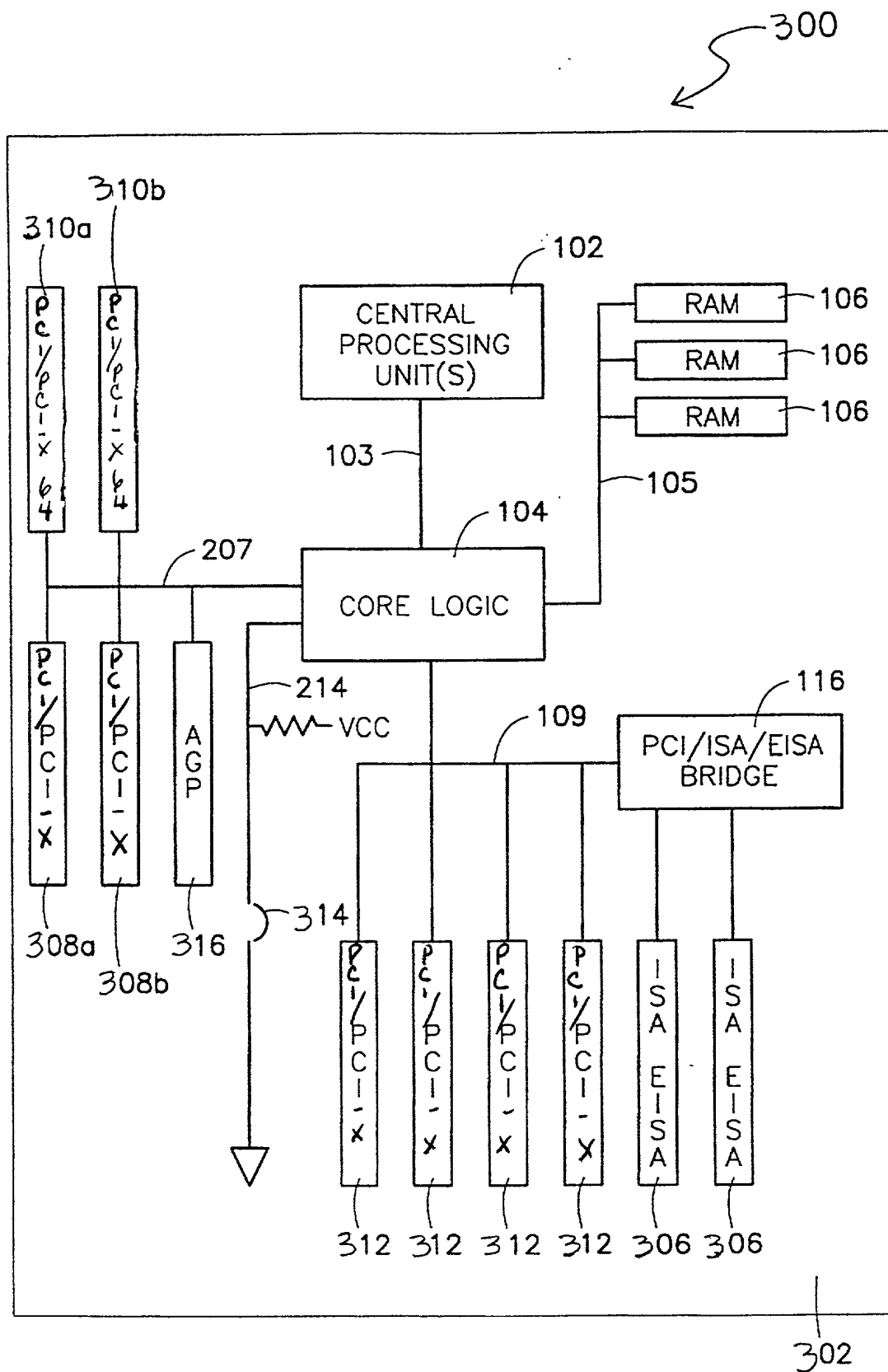


FIGURE 3

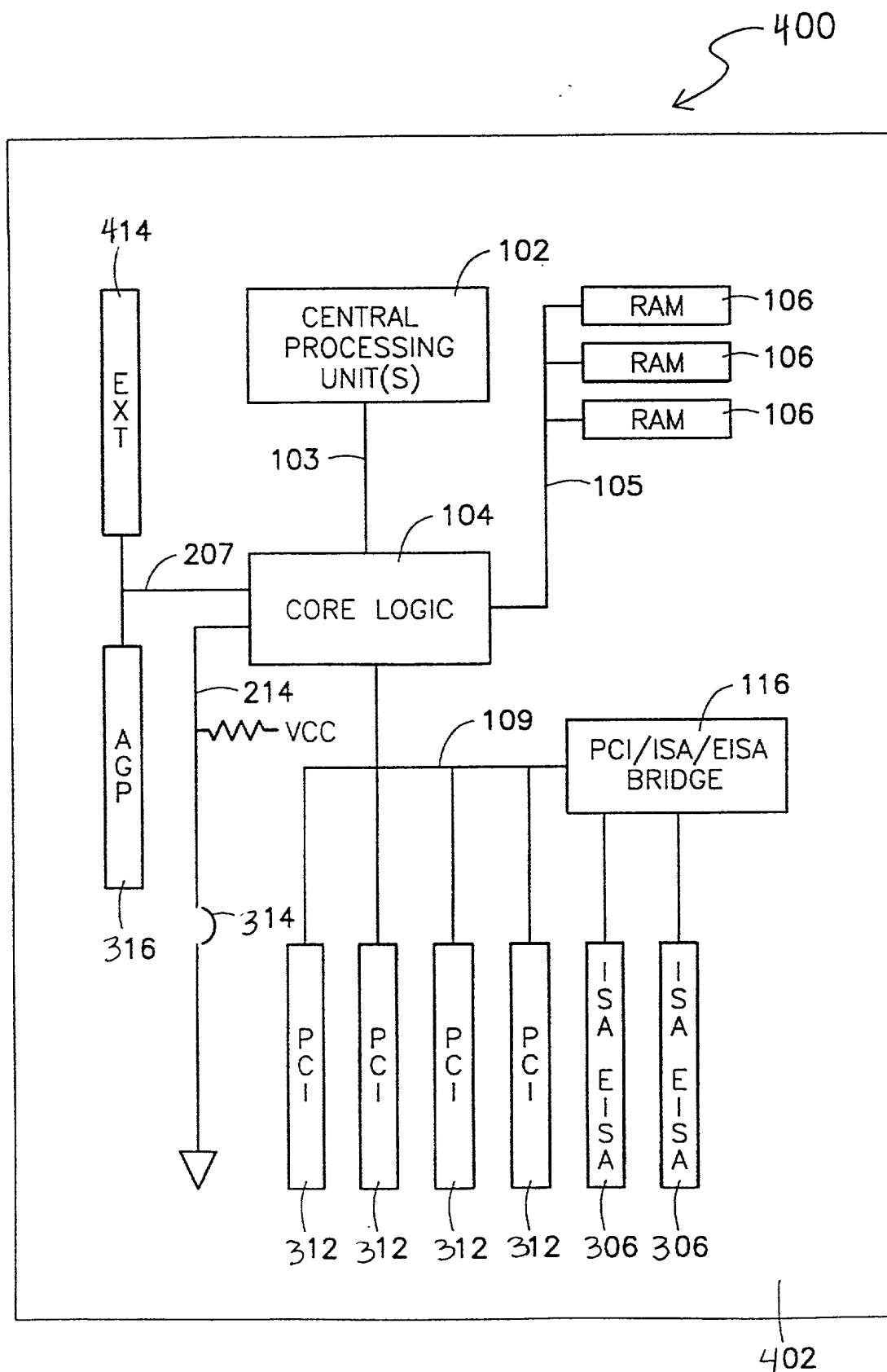


FIGURE 4

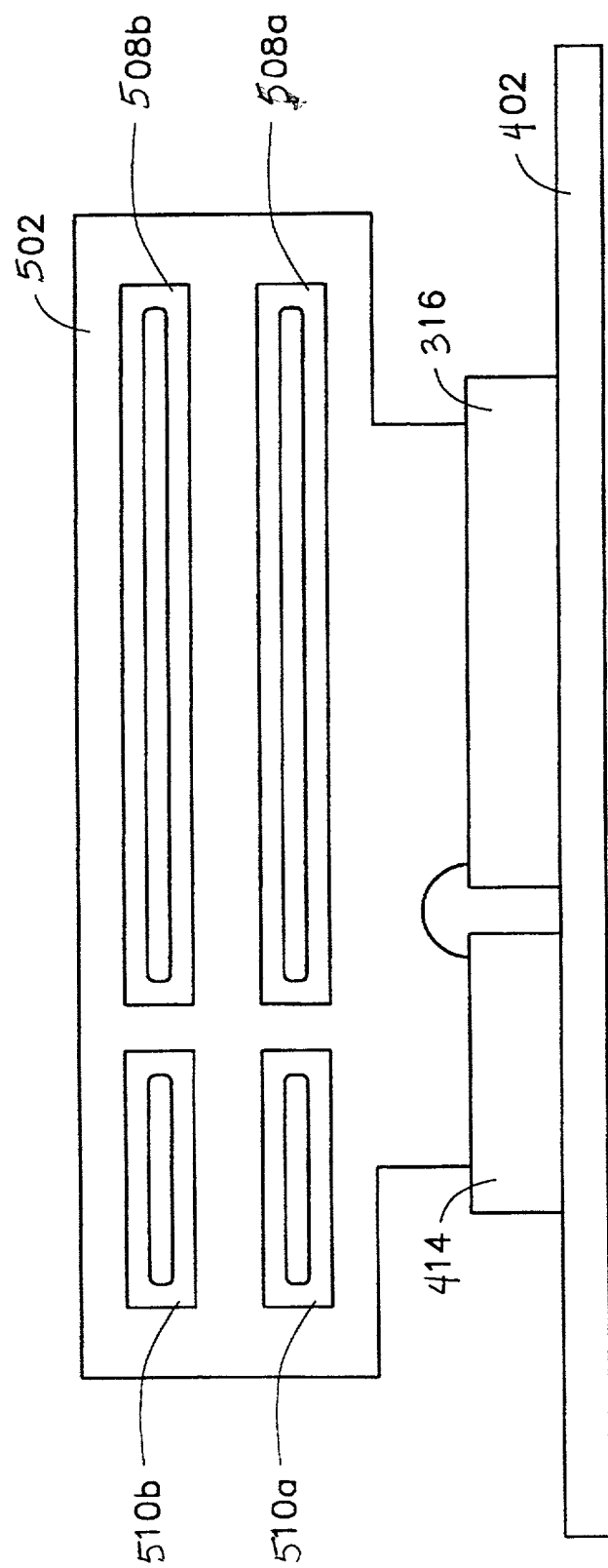


FIGURE 5

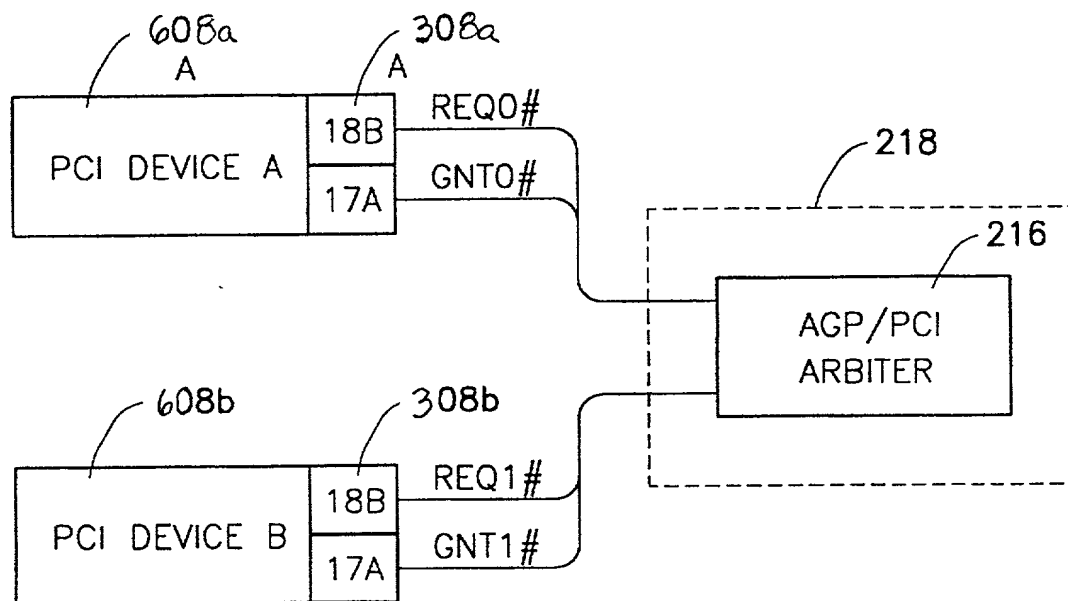


FIGURE 6

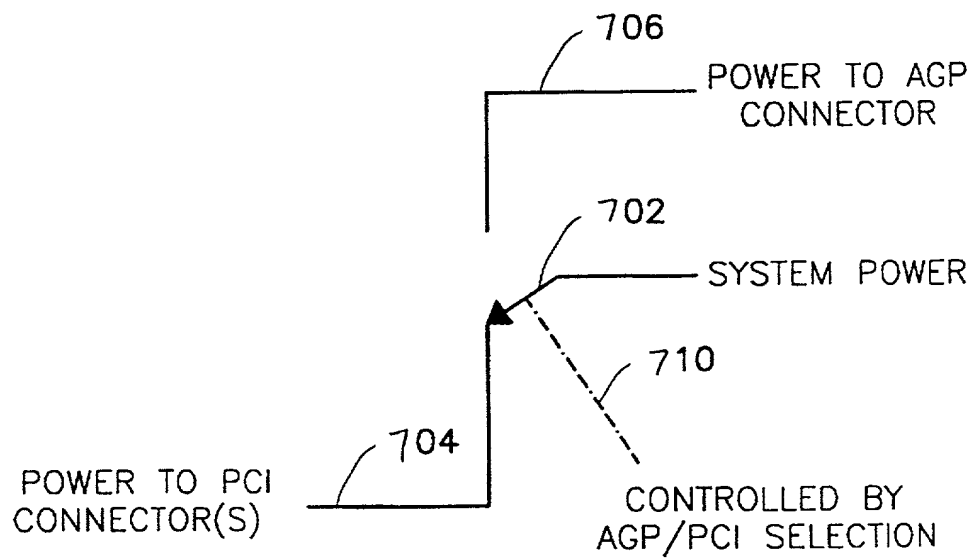


FIGURE 7

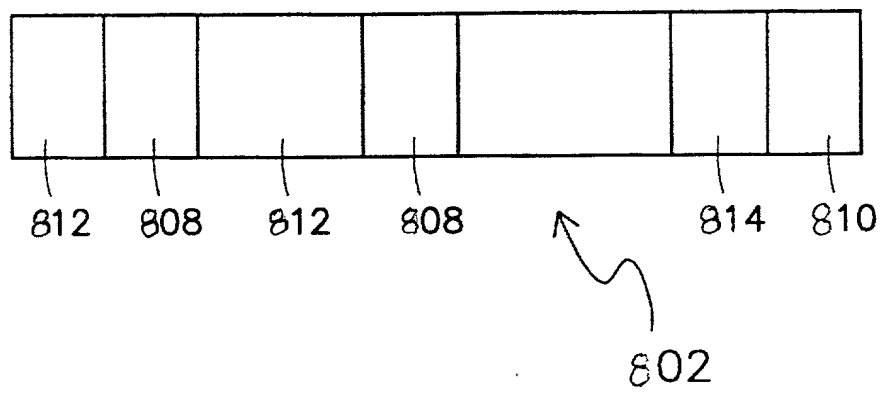
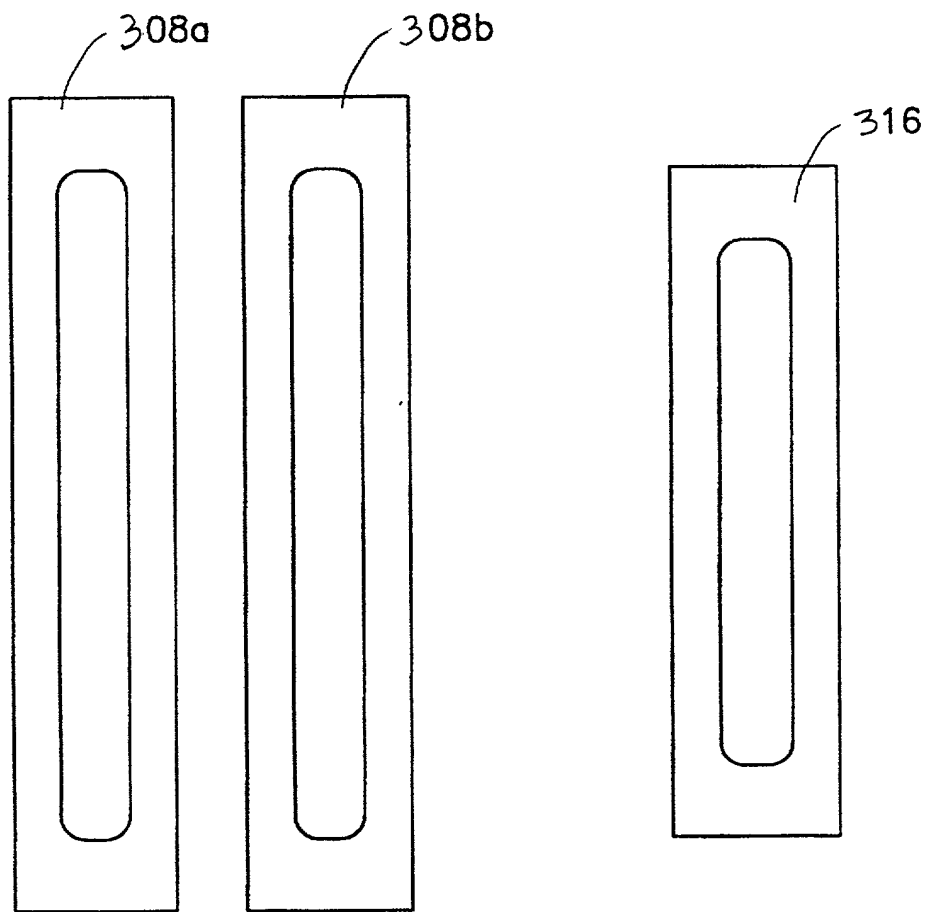


FIGURE 8A



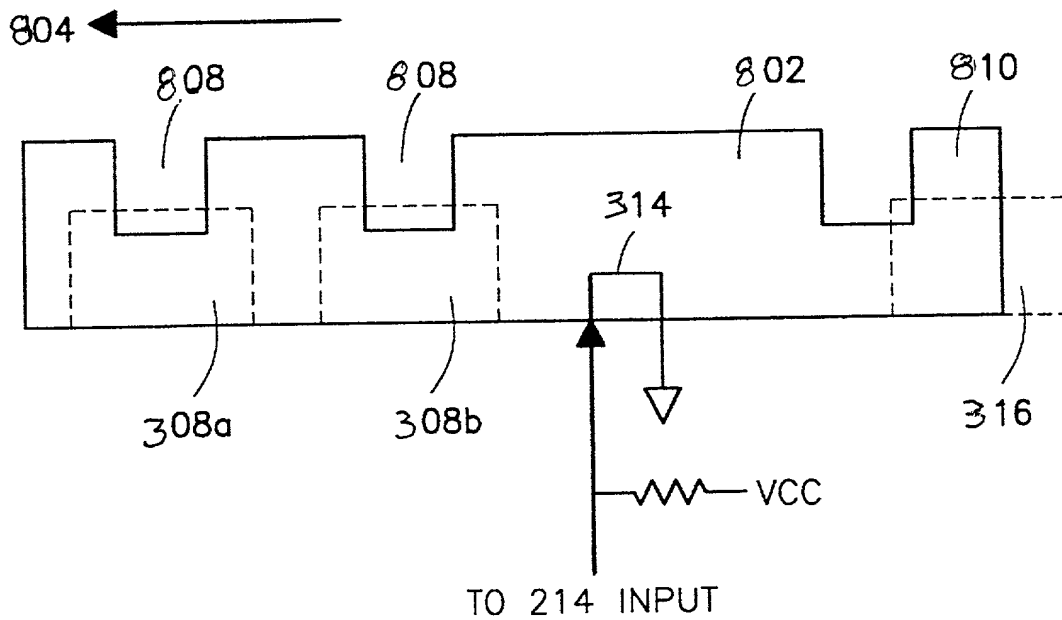


FIGURE 8B

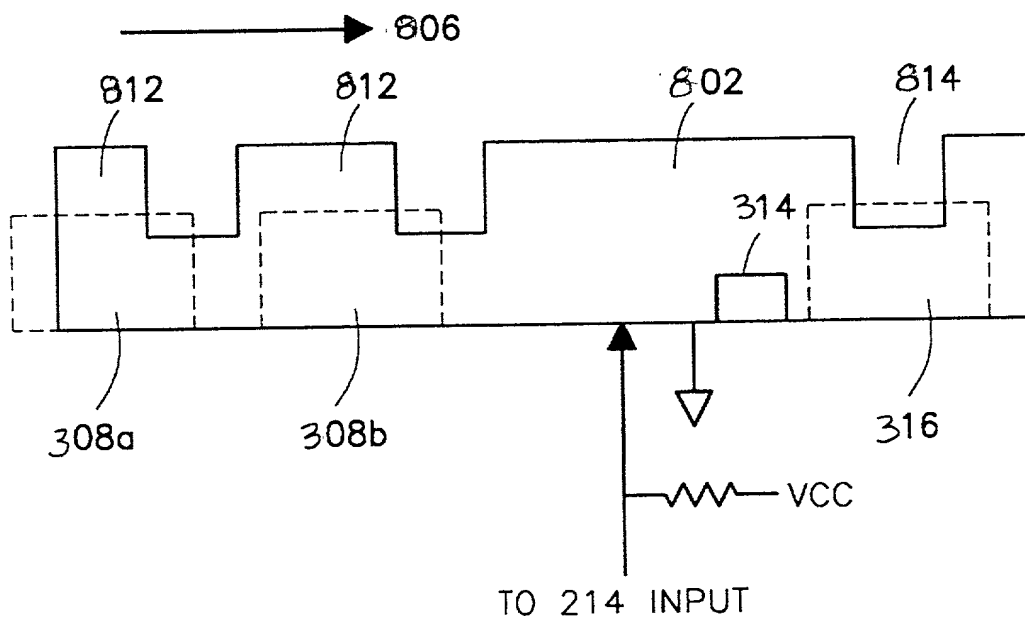


FIGURE 8C

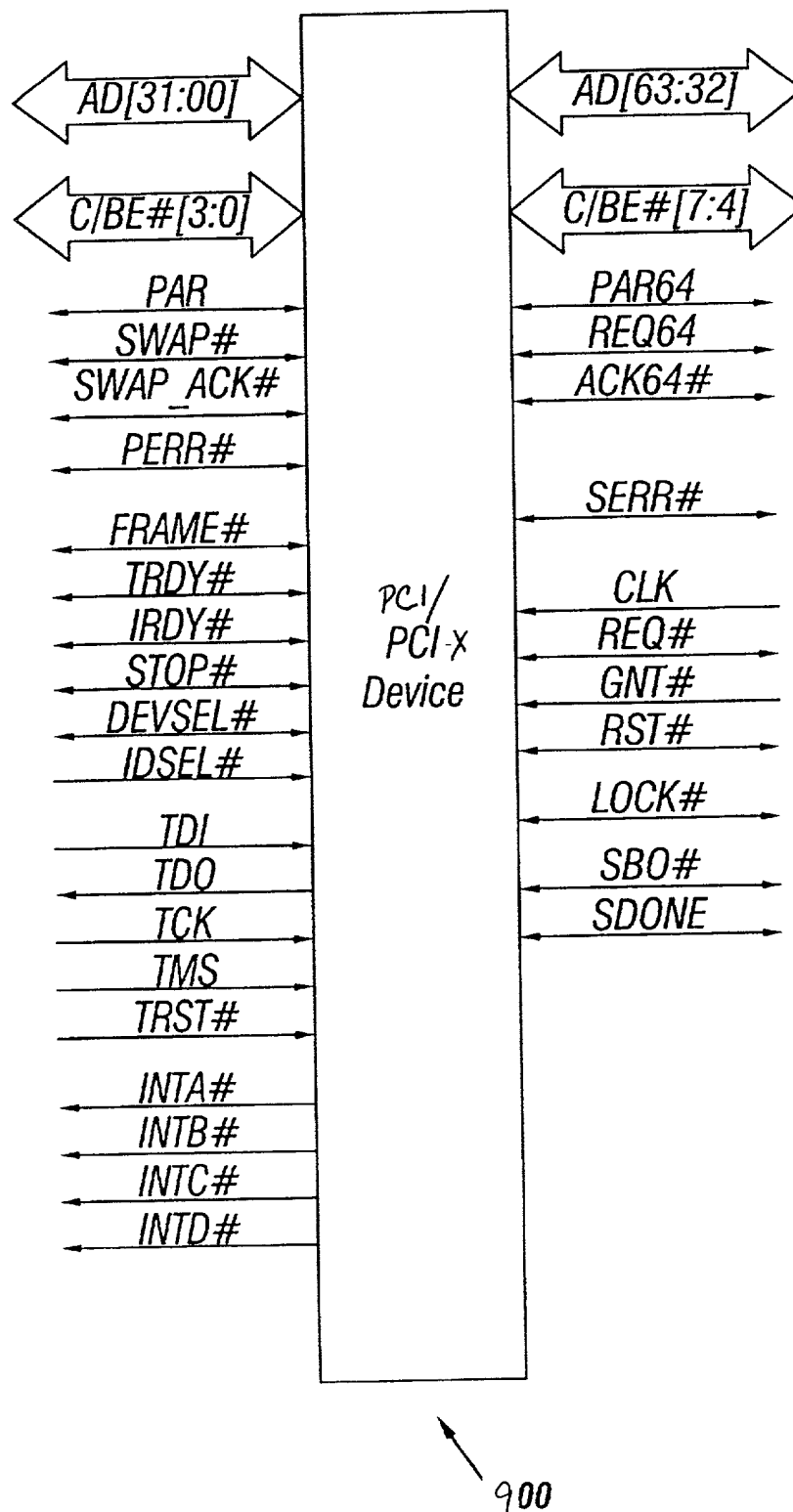


FIG. 9

Byte 3		Byte 2		Byte 1		Byte 0		
Device ID				Vendor ID				00h
Status				Command				04h
Class Code						Revision ID		08h
Bist		Header Type		Latency Timer		Cache Line Size		0Ch
Base Address Registers								10h
								14h
								18h
								1Ch
								20h
								24h
Cardbus CIS Pointer								28h
Subsystem ID				Subsystem Vendor ID				2Ch
Expansion ROM Base Address								30h
Reserved								34h
Reserved								38h
Max_Lat		Min_GNT		Inter. Pin		Inter. Line		3Ch

FIG. 10

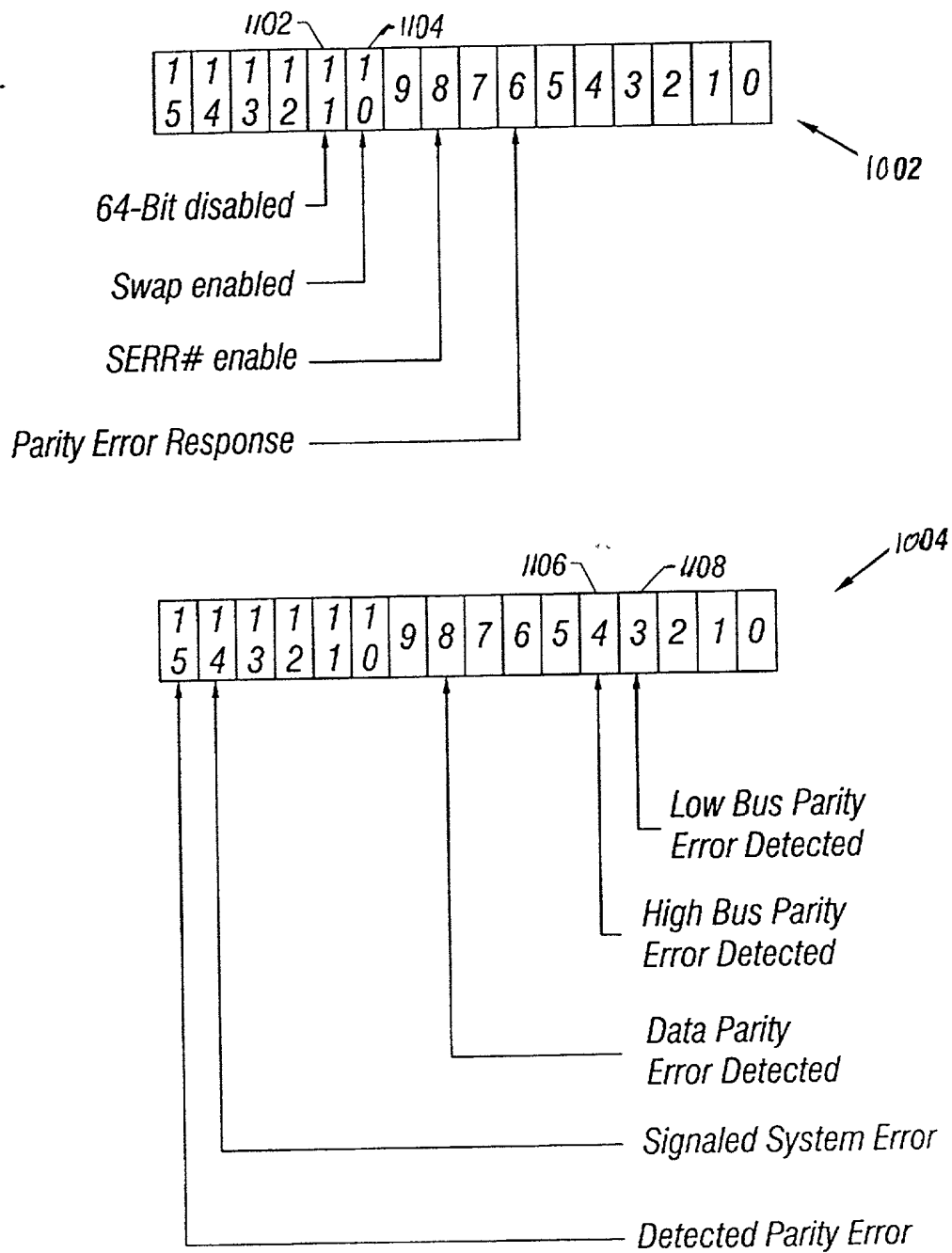


FIG. 11

FIG. 12A is a timing diagram showing the relationship between the CLK, FRAME #, REQ64 #, SWAP #, AD [31:0], CB/E [3:0], PAR, AD [63:32], and CB/E [7:4] signals. The diagram illustrates the sequence of operations and data transfers over time, with the CLK signal providing the clock reference. The FRAME #, REQ64 #, and SWAP # signals are active-low, while the AD [31:0], CB/E [3:0], PAR, AD [63:32], and CB/E [7:4] signals are active-high. The data transfers are shown as sequences of 8-bit data words, with the ADDRESS, CMD, and BEN signals being 8-bit wide, and the DATA, PDATA, and BEN signals being 16-bit wide.

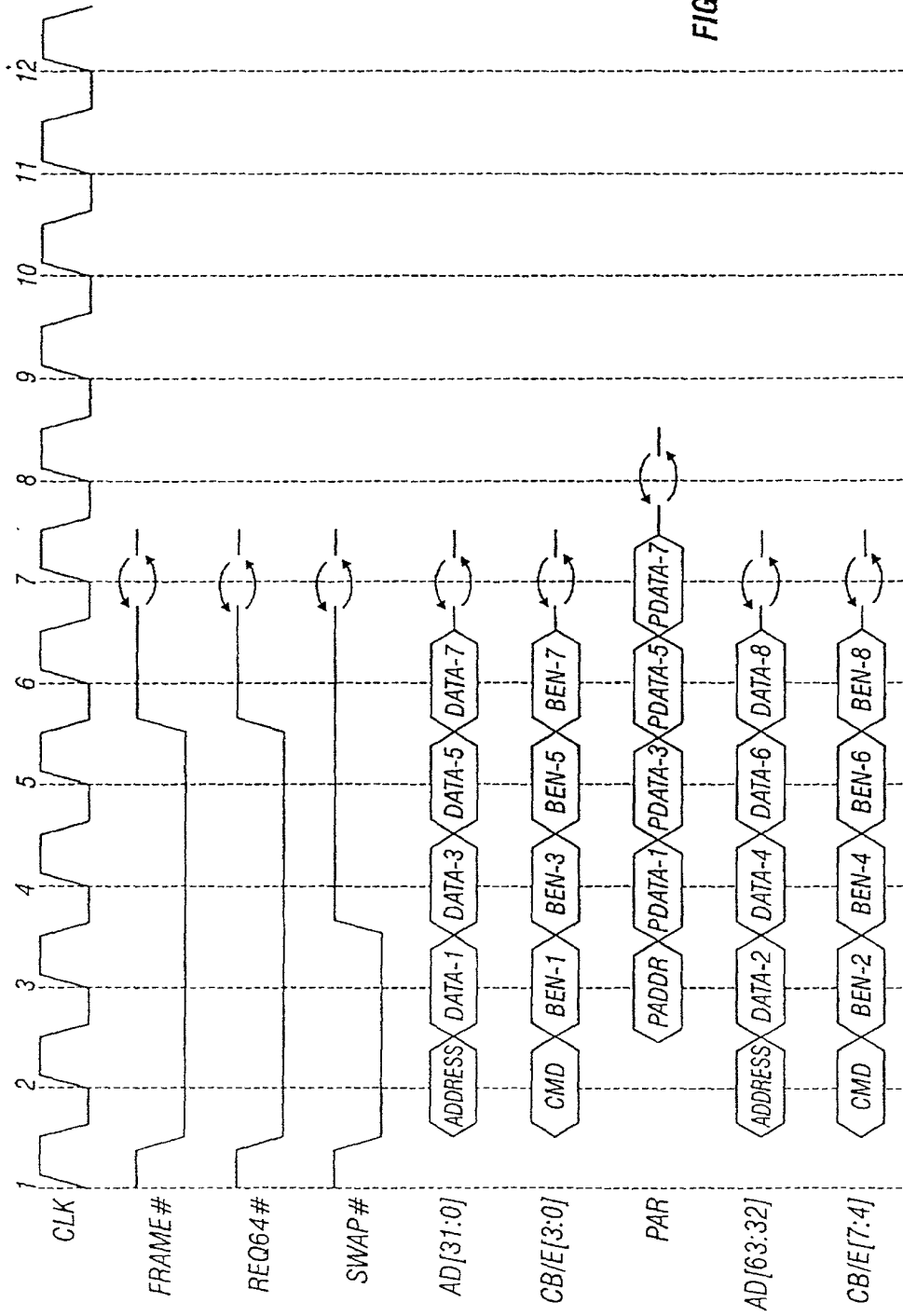


FIG. 12A

FIG. 12B

FIG. 13A is a timing diagram for the data transfer sequence of the present invention. The diagram shows the relationship between the clock signal (CLK) and the various control and data signals. The clock signal is a periodic square wave. The control signals (FRAME #, REQ64 #, SWAP #) are active-low signals that are asserted for a specific duration. The data signals (AD[31:0], CB/E[3:0], PAR, AD[63:32], CB/E[7:4]) are shown as a sequence of data words (DATA-1, DATA-2, DATA-3, DATA-4, DATA-5, DATA-6) and control words (BEN-1, BEN-2, BEN-3, BEN-4, BEN-5, BEN-6) that are transferred over the bus. The diagram illustrates the timing of the data transfer sequence, showing that the data is transferred in a burst mode, with the control signals being asserted before the data transfer begins.

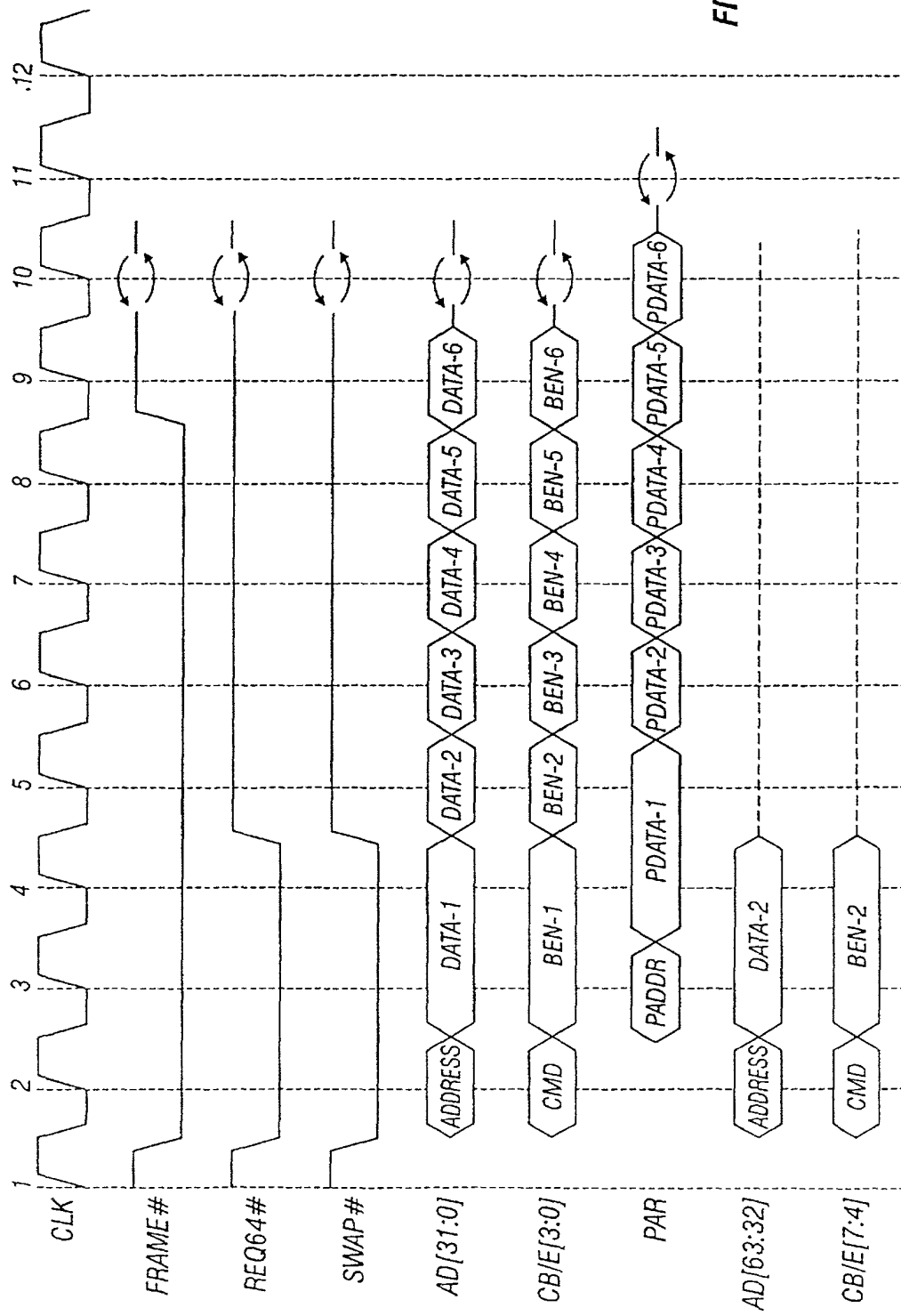


FIG. 13A

FIG. 13B is a timing diagram showing the sequence of events for a data transfer. The diagram is divided into two main sections: a data transfer phase (lines 1-10) and a control phase (lines 11-12). The data transfer phase shows the transfer of data from the host to the device. The control phase shows the transfer of control signals from the device to the host.

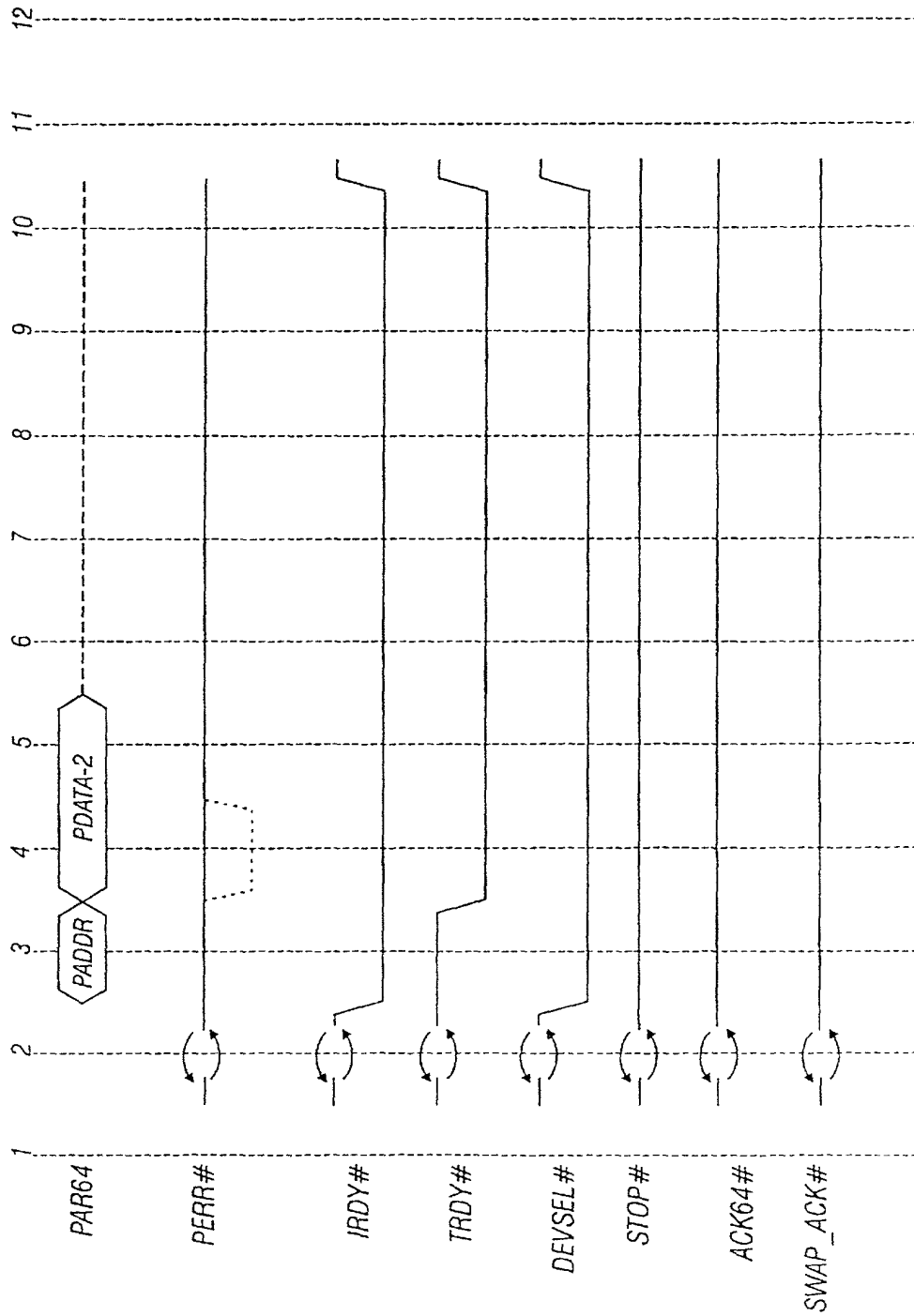


FIG. 13B



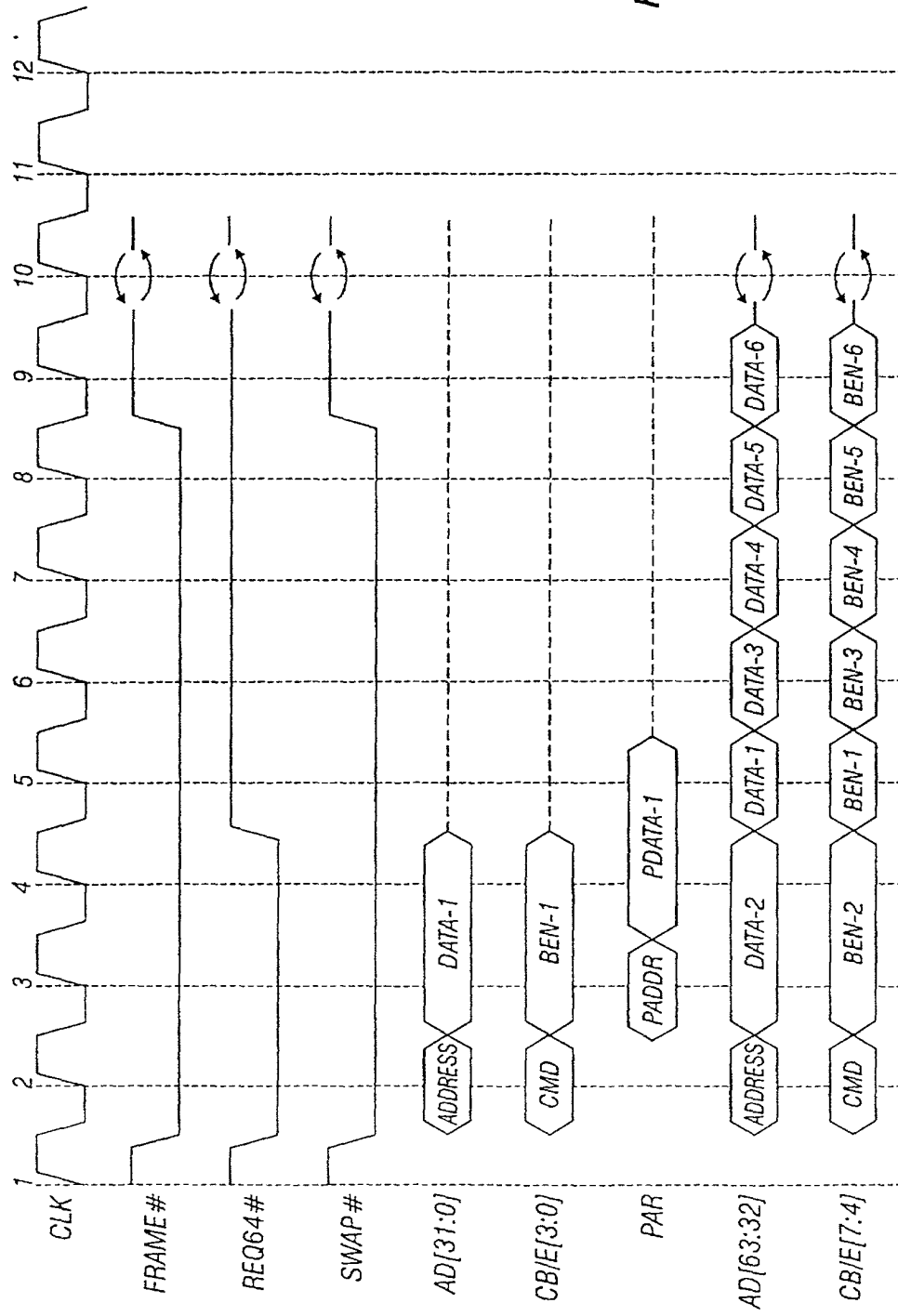


FIG. 14A

FIG. 14B is a timing diagram for the data transfer sequence shown in FIG. 14A. The diagram illustrates the relationship between the data transfer sequence and the timing of the signals PERR#, IRDY#, TRDY#, DEVSEL#, STOP#, ACK64#, and SWAP\_ACK#.

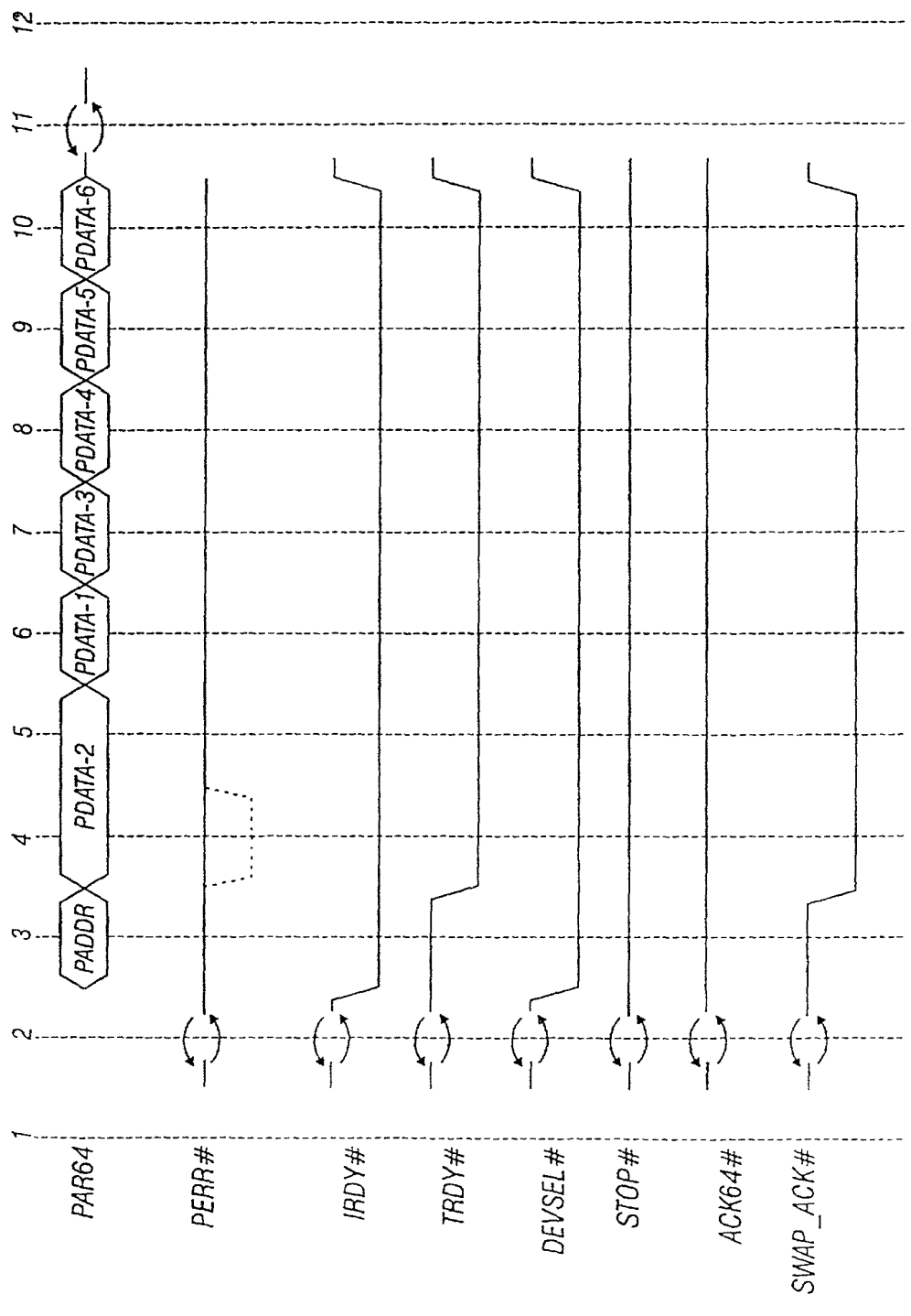


FIG. 14B

FIG. 15A is a timing diagram showing the relationship between the CLK, FRAME#, REQ64#, SWAP#, AD[31:0], CB/E[3:0], PAR, AD[63:32], and CB/E[7:4] signals. The diagram illustrates the sequence of operations for a memory access, including address and data transfer phases.

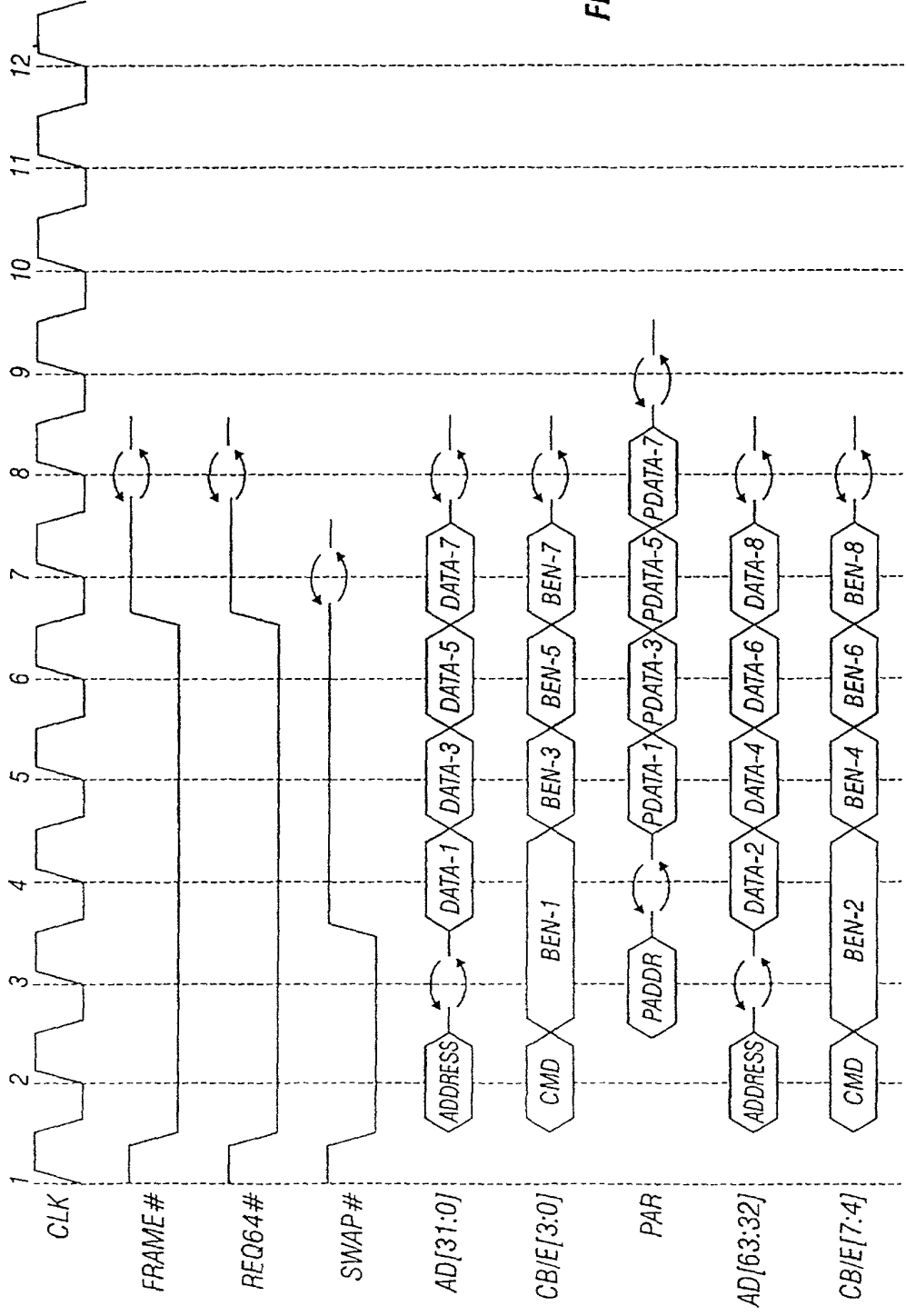


FIG. 15A

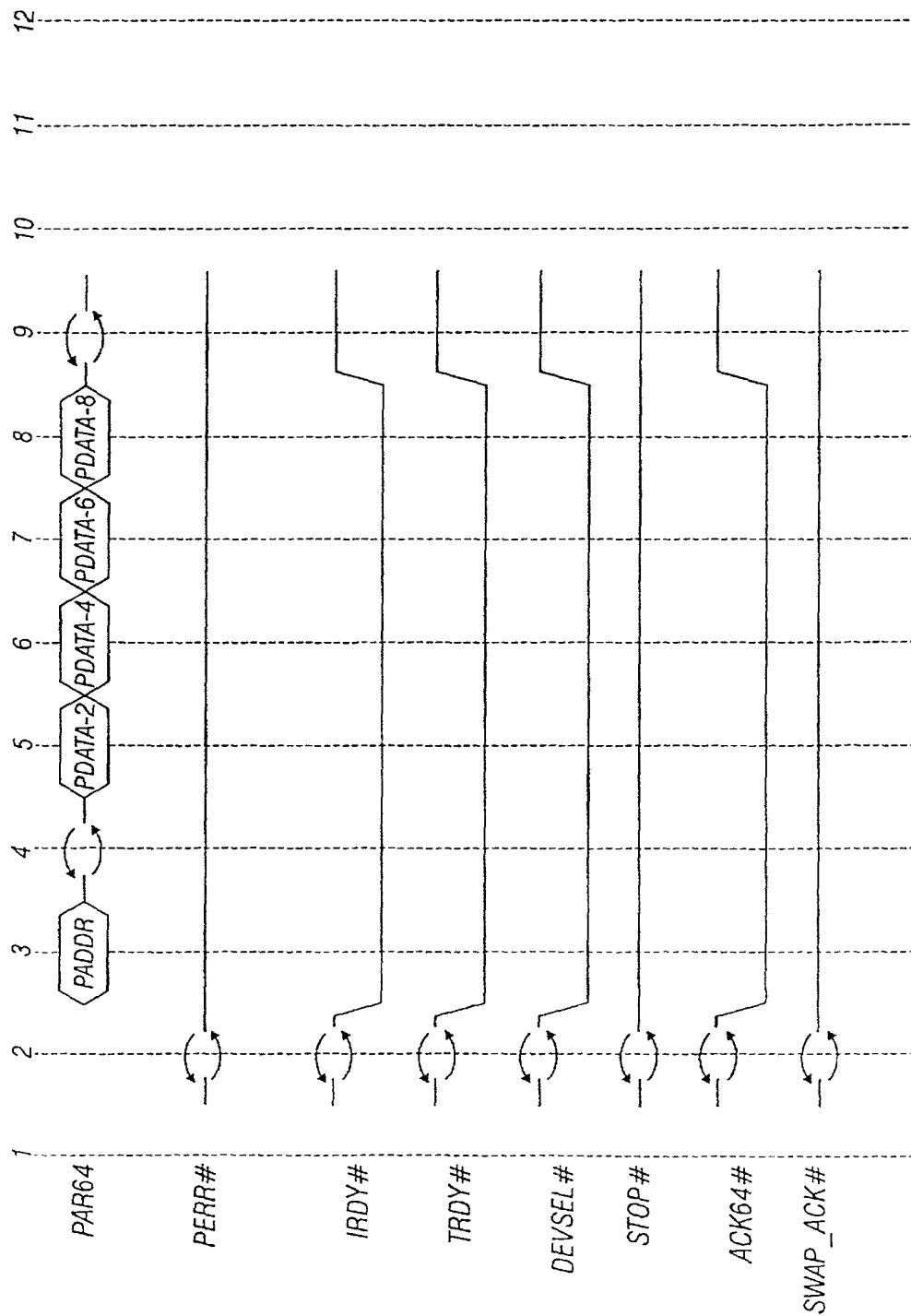


FIG. 15B

The timing diagram illustrates the 64-bit parallel bus protocol over 12 clock cycles. The signals shown are CLK, FRAME#, REQ64#, SWAP#, AD[31:0], CB/E[3:0], PAR, AD[63:32], and CB/E[7:4]. The diagram shows the sequence of operations: ADDRESS, DATA, BEN, PADDR, PDATA, and CMD, with their respective data widths and timing relationships.

FIG. 16A

FIG. 16B

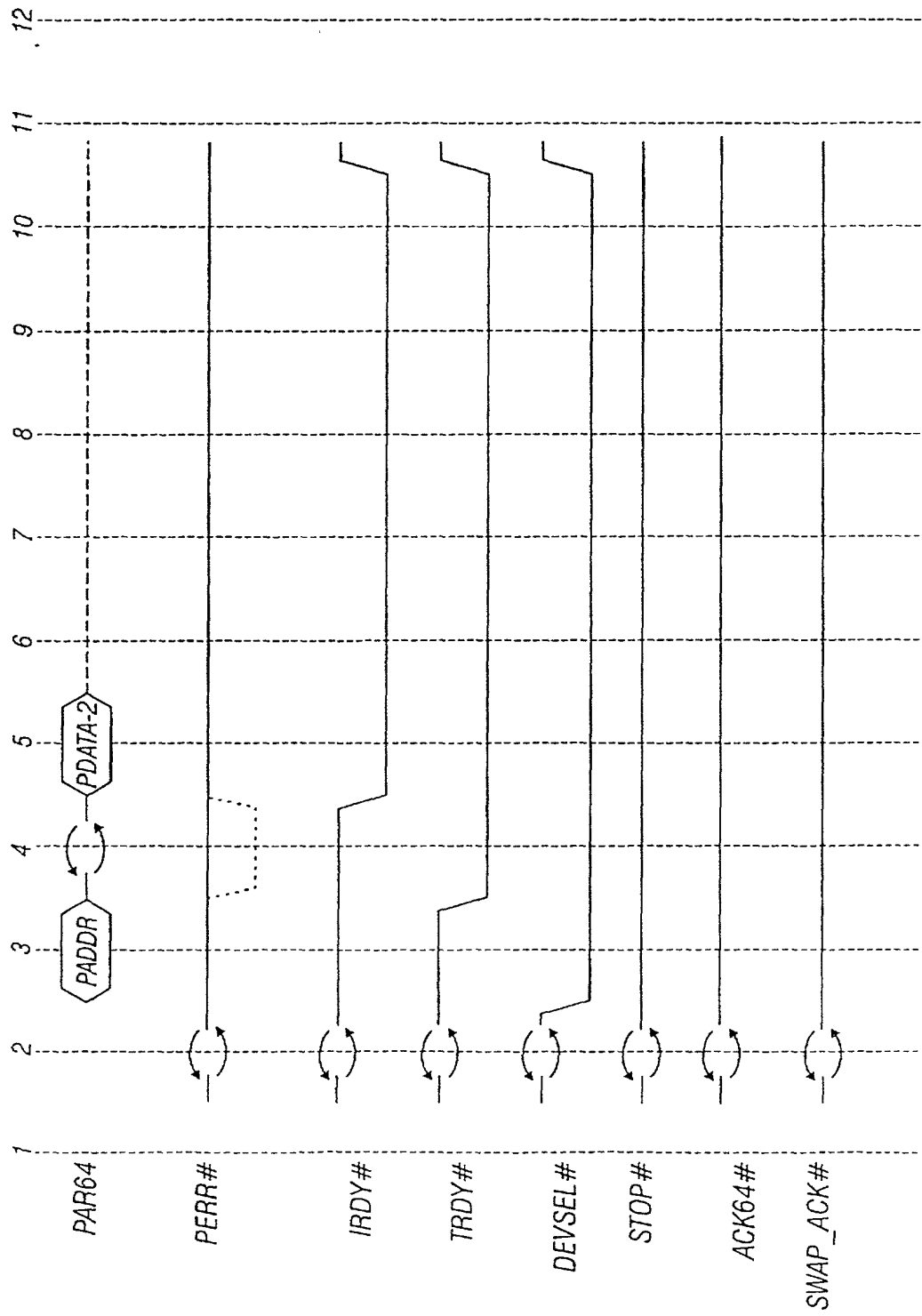
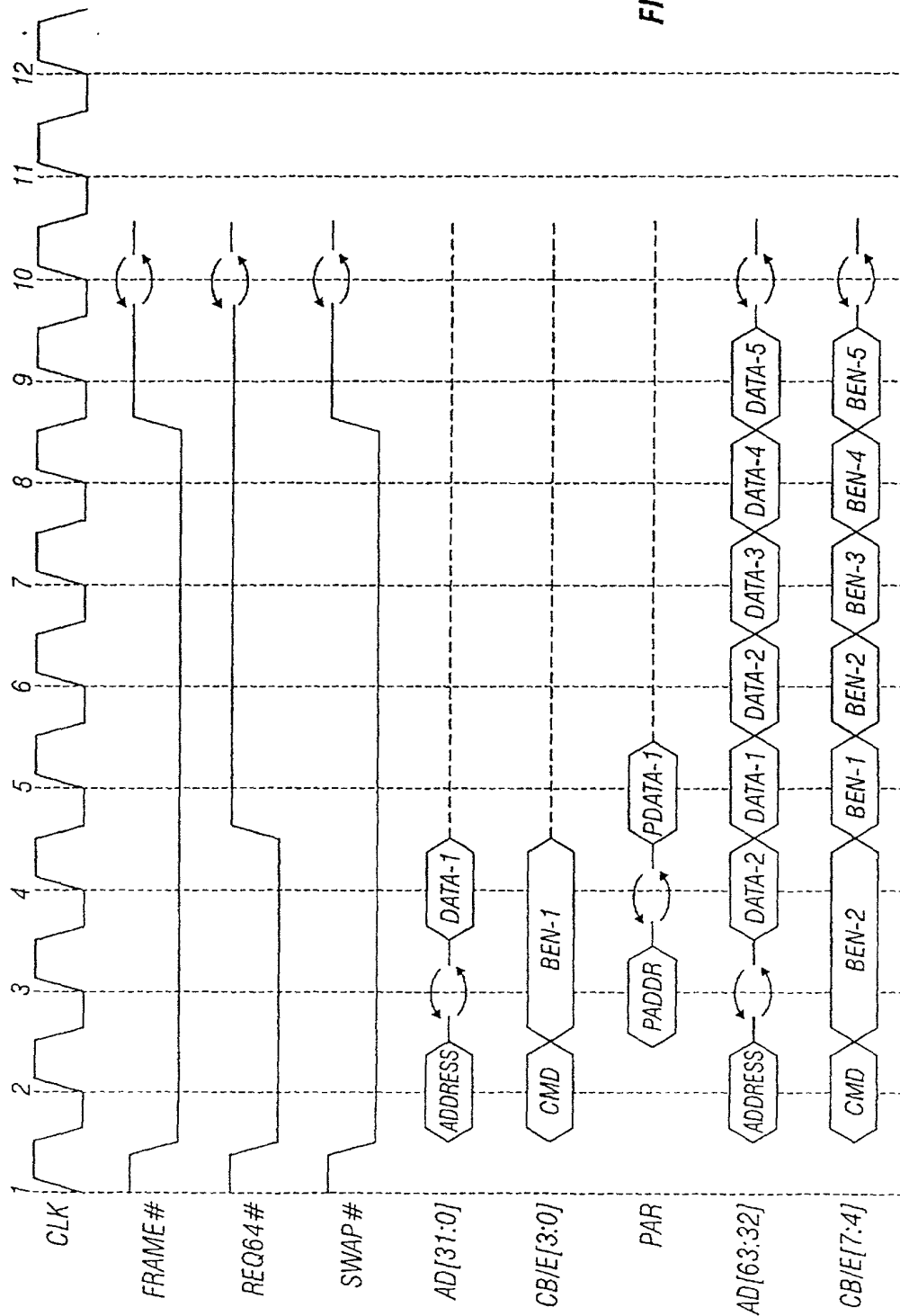


FIG. 16B



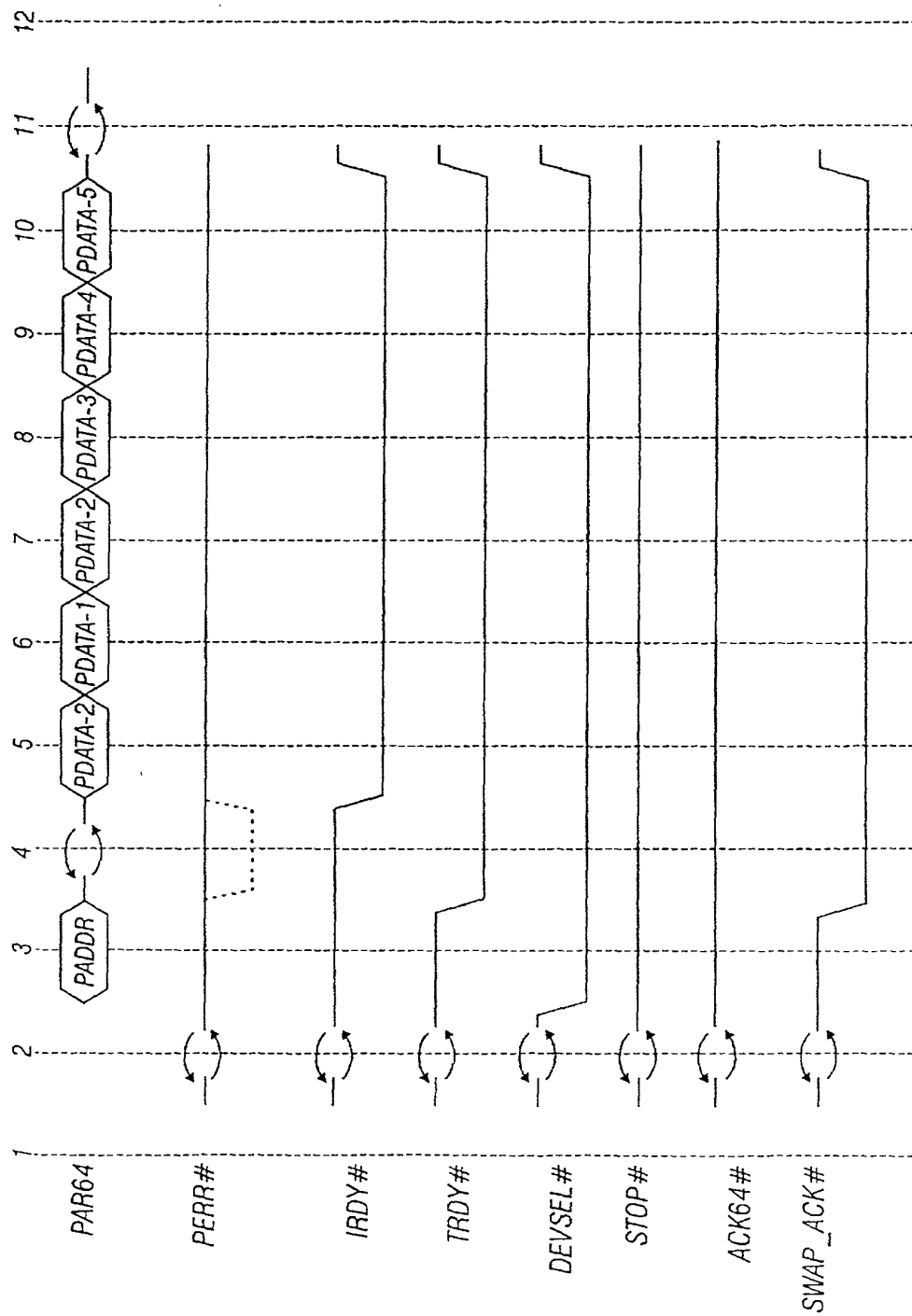


FIG. 17B



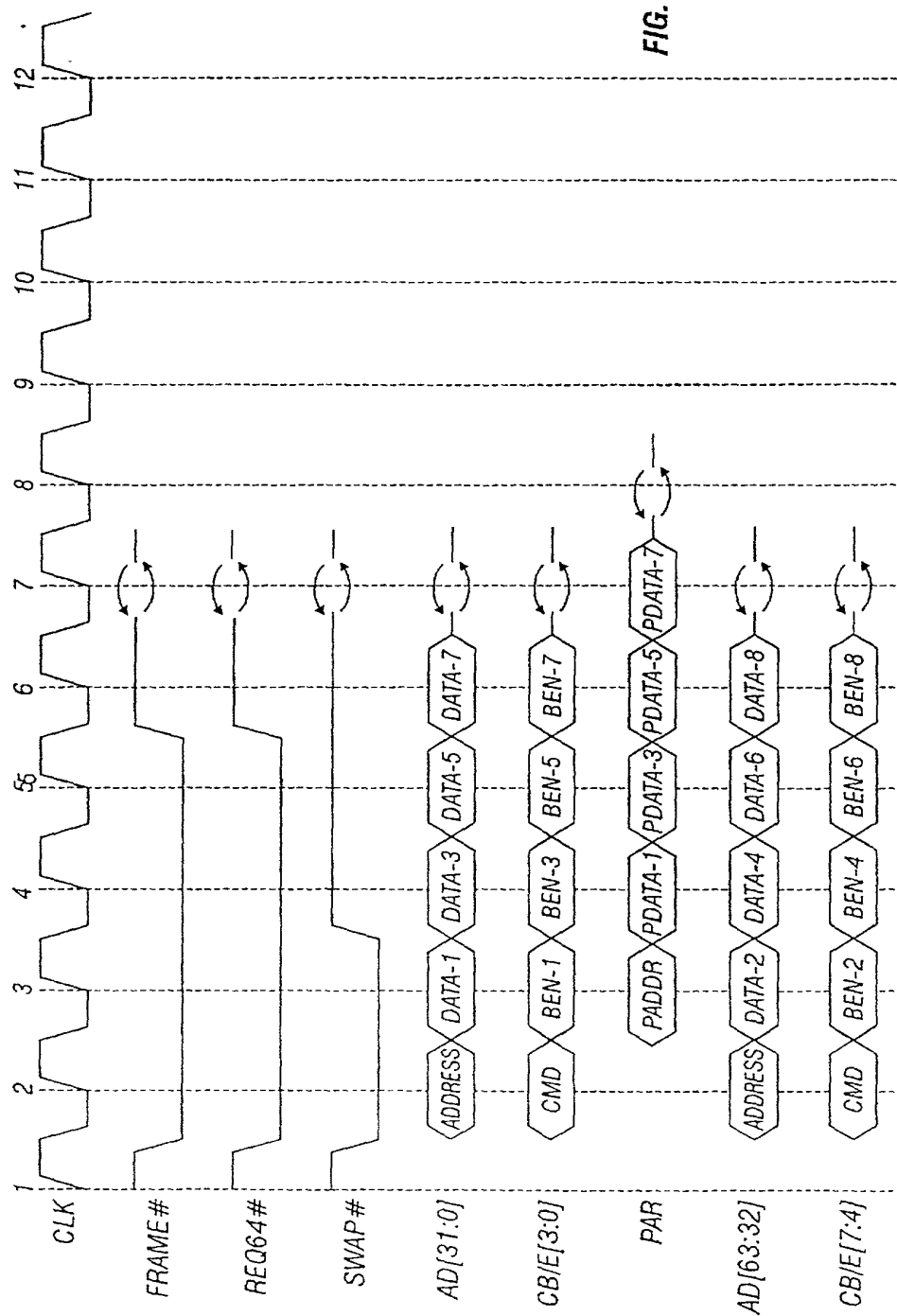


FIG. 108B

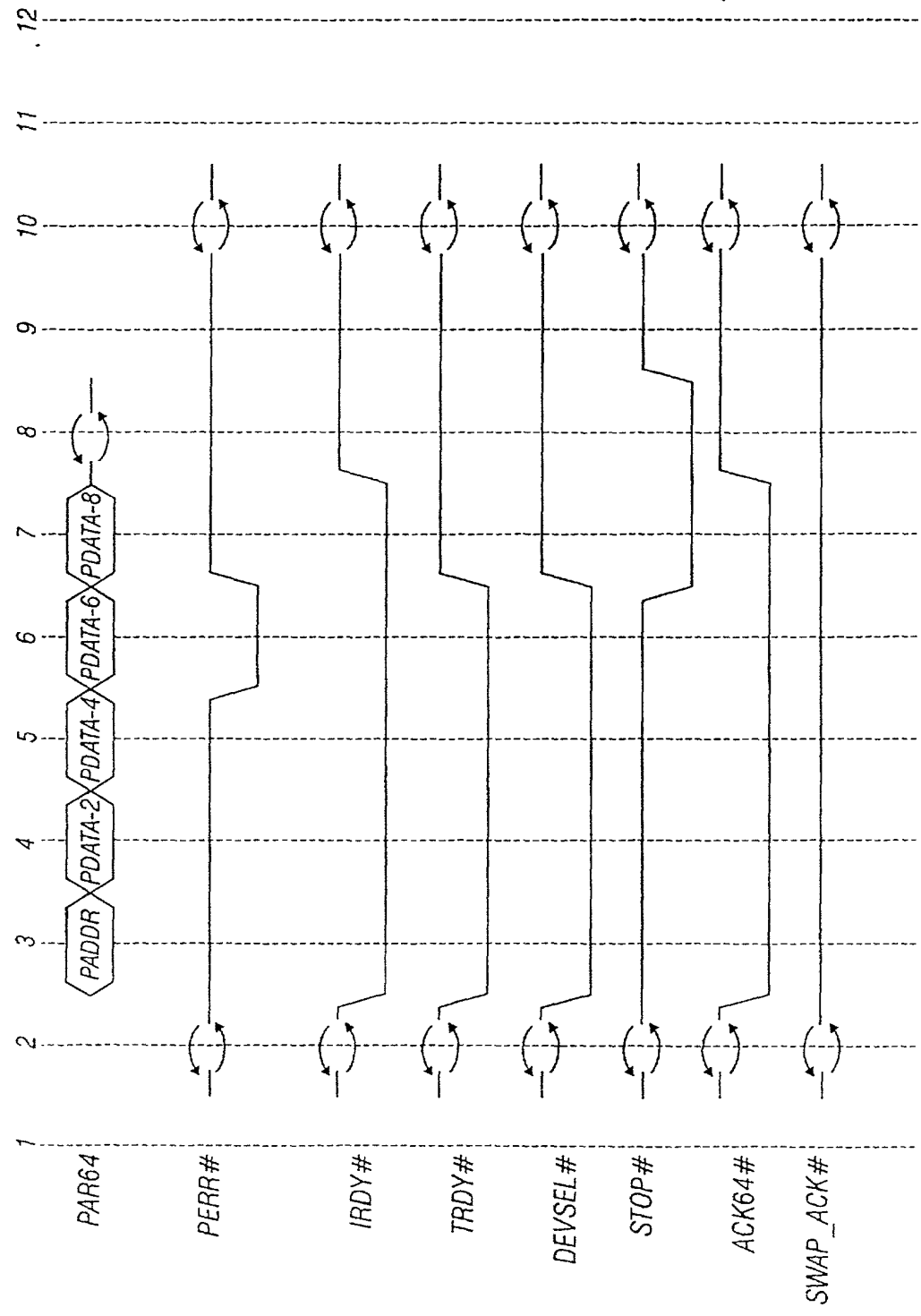


FIG. 108B

FIG. 19 is a timing diagram of a PCI bus cycle. The diagram shows the relationship between the PCI clock (PCL\_CLK) and various PCI signals over 11 clock cycles. The cycle is divided into several phases: PCI Command & Address Phase (cycles 1-4), Extended Command & Attribute Phase (cycles 5-10), Target Response Phase (cycles 11-12), and PCI Turn Around Cycle (cycle 13). The signals shown are AD31:0, AD63:32, C/BE#, FRAME#, IRDY#, TRDY#, DEVSEL#, REQ64#, and ACK64#. The diagram illustrates the sequence of events from the start of the cycle to the termination of the transaction.

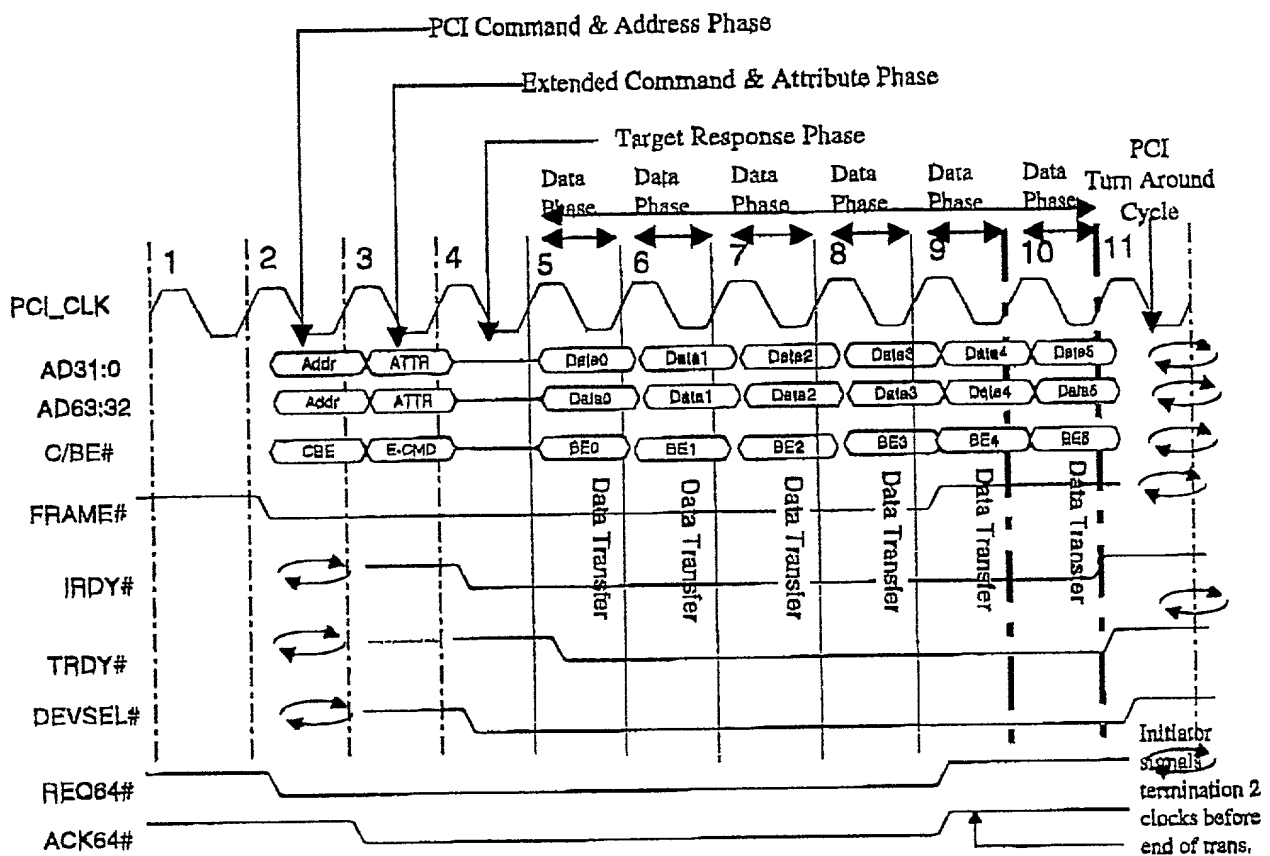


FIG. 19

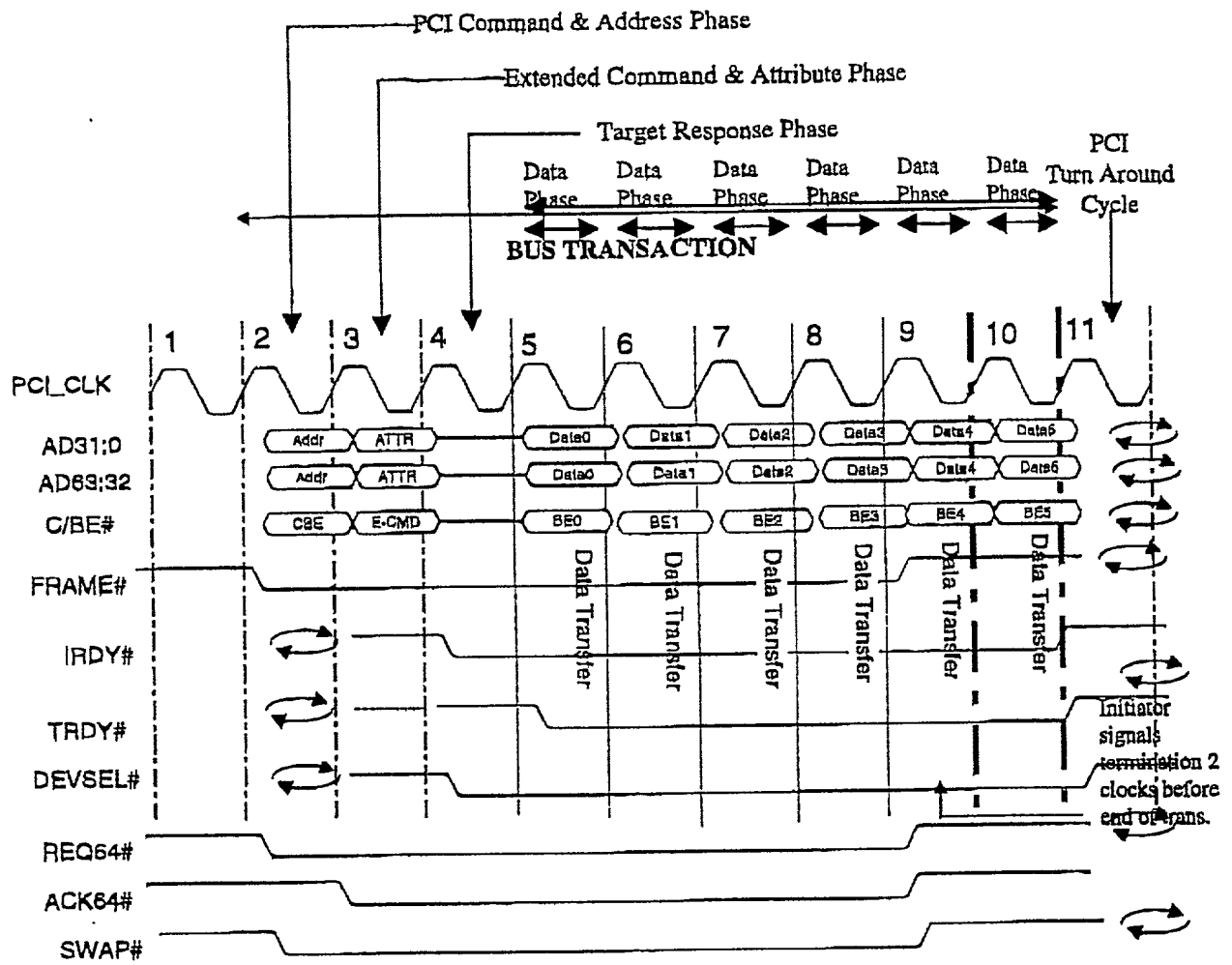


FIG. 20